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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,304	11/12/2003	Janet Teshima	F107	5754

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EXAMINER	
TSAI, CAROL S W	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,304	TESHIMA ET AL.	
	Examiner	Art Unit	
	Carol S. Tsai	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-22 and 28-31* is/are allowed.

6)☒ Claim(s) *1-6 and 23-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/1/04 & 11/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 4, and 5 are rejected under 35 U.S.C. 102(a) as being anticipated by U. S. Patent No. 6,635,872 to Davidson.

With respect to claims 1 and 2, Davidson discloses a defect characterization system that provides rapid feedback for troubleshooting or improving a micro-fabrication process, the system comprising: components for locating defects in a semiconductor wafer, characterizing the defects to determine an appropriate analysis process, and automatically performing the determined analysis process (see col. 3, lines 21-50 and col. 9, line 67 to col. 10, line 14).

As to claims 4 and 5, Davidson also discloses the defects being initially found by an inspection system that creates a defect file, the defect file being used to locate the defects using a high resolution imaging system also used to characterize the located defect to determine the analysis process, the analysis process being automatically carried out by the system (see col. 1, lines 38-55).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davidson in view of U. S. Patent No. 6,337,533 to Hanashi et al.

As noted above, Davidson discloses the claimed invention, except for performing a chemical analysis at the exposed surface.

Hanashi et al. teach the composition content by percentage can be obtained by an analysis in use of an energy dispersion analysis equipment such as EDS.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Davidson's method to include performing a chemical analysis at the exposed surface, as taught by Hanashi et al., because it is well known in the art that a SEM disclosed in Davidson can be accompanied by instrumentation including an energy dispersive x-ray (EDX) detector for performing chemical analysis of the defect.

As to claim 6, Davidson does not disclose cutting multiple cross sectional portions of the wafer and examining said portions with an EDS analysis to provide three-dimension elemental information.

Hanashi et al. teach cutting multiple cross sectional portions of the wafer and examining said portions with an EDS analysis to provide three-dimension elemental information (see col. 7, lines 16-27).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Davidson's method to include cutting multiple cross sectional portions of the wafer and examining said portions with an EDS analysis to provide three-dimension elemental information, as taught by Hanashi et al., in order that each dimension of A, B, d and t of the molten portion can be observed by a microscopic examination (see Hanashi et al. col. 7, lines 23-24).

5. Claims 23-25 and 27 are rejected under 35 U.S.C. 102(a) as being anticipated by U. S. Patent No. 6,539,106 to Gallarda et al. in view of U. S. Patent No. 6,6709,610 to Shemesh et al.

With respect to claims 23-25, and 27, Gallarda et al. disclose a defect analysis system for analyzing defects in a semi-conductor wafer, the system comprising: a charged particle beam for analyzing defects in a wafer (see col. 16, lines 10-34); and at least one processing device with software components to perform analysis on the defect using the at least two charged particle devices; said software components when executed providing a job builder, a sequencer, and a defect explorer (see col. 4, line 61 to col. 5, line 35; col. 6, lines 6-35; and col. 18, line 58 to col. 19, line 22).

Gallarda et al. do not disclose at least two charged particle beams.

Shemesh et al. teach at least two charged particle beams (SEM column 14 and FIB column 12 shown on Fig. 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Gallarda et al.'s method to include at least two charged particle beams, as taught by Shemesh et al., in order that a scanning electron microscope

can be used for generating SEM images and locating a landmark on an object and a focused ion beam miller and imager can be used for locating the landmark on the object and milling the object at a desired location (see Shemesh et al. col. 3, lines 53-56).

6. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. in view of Shemesh et al. as applied to claim 23 above, and further in view of U. S. Patent No. 5,852,793 to Board et al. in view of U. S. Patent No. 2003/0028343 to Velichko et al.

As noted above, Gallarda et al. in combination with Shemesh et al. teach all the features of the claimed invention, but do not disclose a pause tool component that allows the user to define conditions for the analysis process to be halted when executed by the sequencer.

Board et al. teach the program manager providing user interface, graphics, automatic scanning, processing of sensor-related stress wave energy measurements, caution and warning thresholds, user-defined conditions, and selected displays (see col. 11, lines 46-53).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Gallarda et al. in view of Shemesh et al.'s system to include allowing the user to define conditions for the analysis process, as taught by Board et al., in order to indicate when selected sensors have a stress wave energy reading exceeding a predetermined threshold (see Board et al. col. 4, lines 60-62).

Velichko et al. teach an engine control module providing the user interface

feedback on various parametric test system events, and receives parametric test system commands from the user interface in which the user interface providing the operator the ability to issue commands, such as start test, abort, pause, or other commands, to the engine control module (see paragraphs 0022 and 0068).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Gallarda et al. in combination Shemesh et al. and Board et al.'s system to include a pause tool component for the analysis process to be halted when executed by the sequencer, as taught by Velichko et al., in order to issue commands such as an emergency abort, to break test monitor module deadlocks, and to recover from other fault situations (see Velichko et al. paragraph 0068).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kuribara et al. disclose an IC test system analyzing a defective part in the inside of an IC chip.

Shida et al. disclose test patterns being applied to an IC under test under a test pattern address by which the first fail is caused and under other test pattern addresses.

Goishi et al. disclose an IC analysis system having a charged particle beam apparatus in which the operability and picture quality have been enhanced and the measurement method of a device under test.

Levy discloses an electronic component failure indicator for clearly visably indicating on the surface of an electronic component to be tested a self sustaining

indication of the functional operational status of the component.

Harvey et al. disclose a methodology for qualitatively identifying features of an article, such as defects on the surface of a semiconductor substrate, with a string of symbols, such as numbers, according to relevant defect characteristics and information relating to the processing tools visited by the wafer, including reliability information.

Okabe et al. disclose a tool for analyzing by priority a defect having a high possibility of causing an electrical failure when inspecting a particle and a pattern defect in a piece of work which constitutes an electronic device such as a semiconductor integrated circuit, and relates to a system therefor.

Nishi et al. disclose a high-precision transfer stage apparatus for use with lithography apparatuses, instrument apparatuses or other apparatuses and a method for exposing a substrate plate to transcribe circuit patterns and, more particularly, to an exposure apparatus to be used in a lithography process for producing particularly semiconductor devices and liquid crystal display devices and to a stage apparatus for use with such an exposure apparatus, as well as to a method for exposing a photosensitive substrate plate to transcribe device patterns using such an exposure apparatus.

Brankner et al. disclose systems and methods for translating detected wafer defect coordinates to reticle coordinates using CAD data.

Allowable Subject Matter

8. Claims 7-22, and 28-31 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

U. S. Patent No. 6,635,872 to Davidson in view of U. S. Patent No. 6,539,106 to Gallarda et al. and U. S. Patent No. 6,337,533 to Hanashi et al. are references closest to the claimed invention. Davidson in combination with Gallarda et al. and Hanashi et al. disclose a method of characterizing defects in wafers during fabrication in a semiconductor fabrication facility, comprising: (a) inspecting semiconductor wafers to locate defects; (b) storing locations corresponding to the located defects in a defect file; (c) automatically navigating a dual charged-particle beam system to the vicinity defect location using information from the defect file; (d) automatically identifying the defect and obtaining a charged particle beam image of the defect; (e) analyzing the charged particle beam image to characterize the defect; and (h) imaging a surface exposed by the charged particle beam cut to obtain additional information about the defect. However, Davidson in combination with Gallarda et al. and Hanashi et al. do not teach (f determining a recipe for further analysis of the defect; and (g) automatically executing the recipe to cut a portion of the defect using a charged particle beam, the position of the cut being based upon the analysis of the charged particle beam image; and including all of the other limitations in the respective independent claims.

U. S. Patent No. 6,670,610 to Shemesh et al. is the reference closest to the claimed invention. Shemesh et al. disclose a system for analyzing a defect in an object, comprising: (a) an electron beam for imaging the object; (b) an ion beam for milling the object, wherein the electron and ion beams are capable of impacting at a desired location of the object; and (c) a processing device adapted to be communicatively connected to (i) the electron beam for controlling it to image a desired image portion, and (ii) the ion beam for controlling it to mill a desired milling portion. However, Shemesh et

al. do not teach and (d) a computer readable media including instructions that when executed by the processing device cause it to control the system for imaging and milling, identifying a defect using information from a defect file, characterizing the defect based upon an image of the defect formed by the electron or ion beam, removing material based upon the defect characterization to expose a covered portion of the defect, and analyzing the exposed portion of the defect; and including all of the other limitations in the respective independent claims.

U. S. Patent No. 6,539,106 to Gallarda et al. is the reference closest to the claimed invention. Gallarda et al. disclose a defect analysis system for analyzing defects in a semi-conductor wafer, the system comprising: at least two charged particle beams for analyzing defects in a wafer; and at least one processing device with software components for performing analysis on defects in the wafer using the at least two charged particle beams. However, Gallarda et al. do not teach the software components causing the system to (1) automatically relocate a previously identified defect, (2) determine the size and shape of the defect, (3) adjust image magnification of the defect to an appropriate value, (4) adjust charged particle beam parameters, and (5) maintain alignment of the at least two beams as necessitated by changes in beam parameters; and including all of the other limitations in the respective independent claims.

U. S. Patent No. 6,539,106 to Gallarda et al. is the reference closest to the claimed invention. Gallarda et al. disclose a defect analysis system for analyzing defects in a semi-conductor wafer, the system comprising: at least two charged particle beams for analyzing defects in a wafer; and at least one processing device with software

components for performing analysis on defects in the wafer using the at least two charged particle beams. However, Gallarda et al. do not teach the software components causing the system to (1) automatically relocate a previously identified defect, (2) determine the size and shape of the defect, (3) adjust image magnification of the defect to an appropriate value, (4) adjust charged particle beam parameters, and (5) maintain alignment of the at least two beams as necessitated by changes in beam parameters; and including all of the other limitations in the respective independent claims.

U. S. Patent No. 6,539,106 to Gallarda et al. in view of U. S. Patent No. 6,6709,610 to Shemesh et al. arereferences closest to the claimed invention. Gallarda et al. in combination with Shemesh et al. disclose a defect analysis system for analyzing defects in a semi-conductor wafer, the system comprising: at least two charged particle beams for analyzing defects in a wafer having a plurality of dies; a controllable stage for receiving and positioning said wafer relative to the at least two beams; and at least one processing device with software components to perform analysis on the wafer using the at least two charged particle devices. However, Gallarda et al. in combination with Shemesh et al. do not teach said software components providing a job builder to allow a user to define analysis jobs to automatically be performed on the plurality of dies and a sequencer to execute the defined job and cause the system to analyze the dies according to the defined job, said job builder allowing the user to specify a path traveled by the stage for analyzing the separate dies; and including all of the other limitations in the respective independent claims.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

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Art Unit 2857

cswt
July 18, 2005